2. (Unchanged) The display controller of claim 1 wherein said video data comprises luminance and chrominance difference data and said component YUV format comprises a first contiguous block of luminance data and at least a second contiguous block of chrominance difference data.

3. (Unchanged) The display controller of claim 2 wherein said display memory controller receives the first contiguous block of luminance data and stores the first contiguous block of luminance data in at least one byte lane within the display memory.

4. (Unchanged) The display controller of claim 3 wherein said display memory controller receives the at least a second contiguous block of chrominance difference data and stores the at least a second contiguous block of chrominance difference data in at least another byte lane within the display memory.

5. (Unchanged) The display controller of claim 4, wherein said first contiguous block of luminance data comprises one frame of luminance data.

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6. (Unchanged) The display controller of claim 5, wherein said at least a second contiguous block of chrominance difference data comprises one frame of chrominance difference data.

7. (Unchanged) The display controller of claim 6 wherein said at least one byte lane comprises a plurality of pairs of adjacent byte lanes, each pair of the plurality of pairs of byte lanes for storing pairs of luminance data for one line of one frame of video data.

8. (Unchanged) The display controller of claim 7 wherein said at least one byte lane comprises a plurality of pairs of adjacent byte lanes, each pair of the plurality of pairs of byte lanes for storing pairs of chrominance difference data for one line of one frame of video data.

9. (Unchanged) The display controller of claim 8, wherein said chrominance difference data is stored in every other line of each of said plurality of pairs of byte lanes and said display controller further comprises a bit block transfer engine for transferring blocks of data within the display memory, wherein said bit block transfer engine replicates chrominance data from every other line of said

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plurality of pairs of byte lanes to a corresponding adjacent
line within said plurality of pairs of byte lanes.

10.   (Unchanged)   The display controller of claim 9
wherein said bit block transfer engine replicates chrominance
data after said display memory controller has completed
storing one frame of video data in the display memory.

11.   (Unchanged)   The display controller of claim 10
wherein said display controller outputs a signal through said
bus interface to a host processor indicating completion of a
bit block transfer operation.

12.   (Unchanged)   A method for assisting decoding of
video data partially decoded in a host processor, said method
comprising the steps of:
receiving, in a display controller, video data in a
component YUV format in contiguous successive streams of
luminance and chrominance difference data and corresponding
video data addresses within a predetermined address range, and
storing the video data by directing separate luminance
and chrominance difference data into predetermined memory
portions according to a predetermined memory aperture mapped
to a display memory so as to store said video data in a pixel
video format in the display memory.

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13.   (Unchanged)   The method of claim 12 wherein the video data comprises luminance and chrominance difference data and the component YUV format comprises a first contiguous block of luminance data and at least a second contiguous block of chrominance difference data.

14.   (Unchanged)   The method of claim 13 wherein the step of storing comprises the step of storing the first contiguous block of luminance data in at least one byte lane within the display memory.

15.   (Unchanged)   The method of claim 14 wherein the step of storing further comprises the step of storing the at least a second contiguous block of chrominance difference data in a least another byte lane within the display memory.

16.   (Unchanged)   The method of claim 15, wherein the first contiguous block of luminance data comprises one frame of luminance data.

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17. (Unchanged) The method of claim 16, wherein the at least a second contiguous block of chrominance difference data comprises one frame of chrominance difference data.

18. (Unchanged) The method of claim 17 wherein the at least one byte lane comprises a plurality of pairs of adjacent byte lanes, each pair of the plurality of pairs of byte lanes for storing pairs of luminance data for one line of one frame of video data.

19. (Unchanged) The method of claim 18 wherein the at least one byte lane comprises a plurality of pairs of adjacent byte lanes, each pair of the plurality of pairs of byte lanes for storing pairs of chrominance difference data for one line of one frame of video data.

20. (Unchanged) The method of claim 19, wherein the step of storing further comprises the steps of:

storing chrominance difference data in every other line of each of the plurality of pairs of byte lanes, and

replicating, in a bit block transfer engine within the display controller, chrominance data from every other line of the plurality of pairs of byte lanes to a corresponding adjacent line within the plurality of pairs of byte lanes.

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21. (Unchanged) The method of claim 20 wherein the bit block transfer engine replicates chrominance data after the display memory controller has completed storing one frame of video data in the display memory.

22. (Unchanged) The method of claim 21 further comprising the step of outputting a signal to a host processor indicating completion of a bit block transfer operation.

REMARKS

The specification has been amended to correct a minor typographical error. Accordingly, the Applicant respectfully requests that the above amendment to the specification be approved. The Applicant submits that no new matter has been added by virtue of the above amendment to the specification.

Claims 1-22 are rejected under 35 U.S.C. Section 103(a) as allegedly being unpatentable over by U.S. Patent No. 5,604,514 to Hancock ("Hancock '514") in view of U.S. Patent

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